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PATENT APPLICATION
SERIAL NO. 10/733,840

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chow et al.

Serial Number: 10/733,840

Filed: December 11, 2003

For: METHOD FOR HIDING LATENCY IN A
TASK-BASED LIBRARY FRAMEWORK FOR A
MULTIPROCESSOR ENVIRONMENT

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Confirmation No.: 2185

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Examiner: Camquy Truong

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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on: November 2, 2007

/Bradley D. Ellis/
Bradley D. Ellis

RESPONSE

In response to the Office Action mailed August 03, 2007 ("Office Action"), Applicants respond as follows: